

PCB 75022

13.1 Introduction

This card takes the audio input signal and provides four microcomputer-selected d.c. rectified characteristics that comply with the commonly-used standards; namely, peak programme meter (PPM), quasi-peak (CCIR 468-2), average-responding scaled for the RMS value of a sine wave (AVG) and true RMS. After rectification and selection, the chosen characteristic is suitably attenuated so that each applies the same d.c. output to the meter drive circuit. The circuits are so designed to ensure that the frequency response characteristics are independent of signal levels.

The 468-2 requirement is that the overload margin of the measuring arrangement, including rectifiers, must be at least 30 dB. The nominal input voltage applied to the rectifier card is -10 dBu, with a maximum 'clip' in excess of +20 dBu to allow for this requirement. However, for the remainder of the rectifier characteristics (i.e. RMS, PPM, AVG) the pre-rectifier a.c. gain is increased and post-rectifier gain decreased in order to further minimise the effects of offset voltages and dependence of frequency response in signal level.

The output switching and attenuation circuit is also wired to accept the phase input and three separate d.c. input options (W&F, IMD and spare). If fitted, these circuit card options provide a d.c. output level of 1 V for 0 dB or 77.5 % of full scale deflection.

In addition, the card provides a buffered oscilloscope output monitoring the audio input signal to the meter. The phase at this output can be reversed under microcomputer control in order to compensate for phase reversals arising from different function selections, thereby ensuring that the oscilloscope output is always in phase with the input signal.

A buffered output is also provided for aural monitoring purposes.

Figure 13.1.1 below shows the block diagram of the card.



13.2 Circuit Description

13.2.1 Input buffer

The audio signal is input on SKT1/4 to the high impedance input of the amplifier IC1, which has low a.c. gain, preset by VR1. When PPM is selected (logic 0 on driver pin IC11/11) the frequency compensation network R5, C3 is short-circuited by analogue switch IC11/12,14. Thus, the signal on output IC1/6 is applied via R4//R6 to coupling capacitor C10.

13.2.2 Multiplexer Outputs and Control Inputs

The rectifier selection multiplexers IC13, IC14 are identical 8-channel analogue switching devices with three encoded microcomputer-controlled inputs A, B and C. These control logic inputs are applied via a non-inverting level-shifter, IC15. The logic inputs for the different rectifiers are shown in table 13.1.

Note that the control line for reducing the pre-rectifier gain, on the anode of D13, is only at logic 1 when the 468-2 rectifier is selected; i.e., when only the A control input is at logic 1. When either the B or C input is at logic 1 (or both), transistor TR5 short-circuits D13 anode to earth (logic 0).

Diode D15 is clamped to TR5 collector to ensure that the 468-2 output on IC13/14 does not exceed +13 V and thereby interfere with the correct operation of IC13 when rectifiers other than 468-2 are selected.

When one of the eight switches of IC13 is selected, its input is connected via the common output IC13/3 to the non-inverting input of the output amplifier IC7b.

An identical 8-channel multiplexer, IC14, also controlled by inputs A, B and C, is connected in the negative feedback path of IC7b to select preset resistor values (VR6 to VR10) for the different rectifiers. These resistor networks enable individual gain presetting for the different rectifiers so that the output voltage remains the same regardless of which is selected.

The PHASE and three option inputs (SKT3/1,2,3,4) are each designed to give a d.c. input of 1 V for 0 dB or 77.5 % of full scale deflection and therefore share the same output gain preset, VR10.

The active 'high' pulse DISCHARGE PEAK DETECTORS input on SKT4/2 is applied via level shifter IC15/5,4 to turn-on transistors TR3, TR4 momentarily, in order to discharge capacitors C14 and C15.

Normally, the card output is directly connected to the meter driver circuit via IC12/12,14. However, when the logic input LOG/LIN on SKT4/1 is high, a logic 1 is applied via IC15/7,6 to analogue switch driver input IC12/11. Switch IC12/14,13 now connects the meter drive output on SKT2/5 to the input from the LOG LAW CONVERTER output via SKT2/6, so that the card output is now routed via the log law converter to the meter drive circuit.

Logic Input Tables

Table 13.1

Function/Rectifier Selection	Control Inputs		
	A (SKT 4/6)	B (SKT 4/5)	C (SKT4/4)
PPM	0	0	0
QUASI-PEAK	1	0	0
AVG	0	1	0
RMS	1	1	0
W & F	0	0	1
IMD	1	0	1
PHASE	0	1	1
SPARE	1	1	1

Table 13.2

SCALE	LOG/LIN (SKT4/1)
dB NORM	1
dB EXP	1
% DIST/VOLTS	0

Table 13.3

FUNCTION	SCOPE MON PHASE (SKT 4/3)
X-TALK	0
THD	0
LEVEL	1
READ-OSC	1
IMD	N/A
W & F	N/A

13.2.3 Rectifier Circuit

The audio output from C10 is applied to integrated circuits IC3, IC4 and IC5, which serve to give high-speed full-wave rectification.

The positive-going half-cycles of the input signal at the inverting input IC3/2 result in negative-going half-cycles on output IC3/6, which are blocked by D1, but passed via R20 and diode D2 to the junction of R19 and R22. Resistor R19 provides the negative feedback to inverting input IC3/2 and R22 passes the negative-going half-cycles to inverting input IC5/2. These alternate half-cycles result in corresponding positive-going half-cycles at output IC5/6.

The negative-going half-cycles of the input signal at the inverting input IC3/2 result in positive-going half-cycles on output IC3/6, which are blocked by D2, but passed via D1 and R21 to the inverting input of IC6, which acts as a current inverter. The resultant current flowing in input resistor R21 is inverted by R23, R24 and IC4 and flows into the node at IC5/2 to give a negative-going current into IC5/2. These alternate half-cycles result in corresponding positive-going half-cycles at output IC5/6 to complete the full-wave rectification process. The network R25, C11, across IC5 inputs, provides a degree of output frequency compensation for stability.

13.2.4 First Peak Detector

Op amps IC6 and IC7a form a fast, accurate quasi-peak detector circuit as required by the PPM and CCIR 468-2 recommendations.

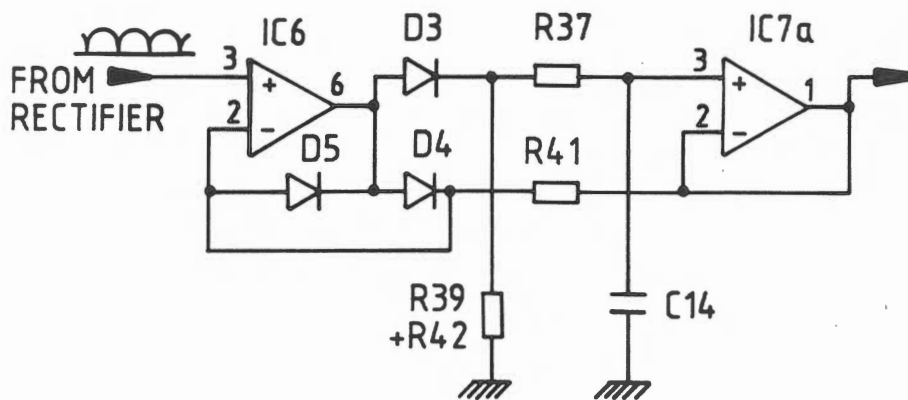


Figure 13.2.1 First peak detector - Simplified circuit

The output voltage at IC7a/1 is always identical to that on C14. When the input voltage at IC6/3 exceeds that on C14 and IC7a/1, IC6/6 goes positive to cause current to flow in D4 and R41. Since D3 and R37 are identical to D4 and R41, equal currents flow through R41 and R37. The voltage at the left end of R37 is therefore held, by the negative feedback around IC6, at a voltage equal to the input voltage.

When the input voltage drops below the voltage on C14, IC6 output goes negative until D5 conducts to maintain the voltage at IC6/2 equal to that on IC6/3. D3 and D4 do not conduct. C14 can only discharge through R39 and R42.

The effective values for the charge, feedback and discharge resistors for C14 are modified by analogue switch sections within IC11 and IC12, to effect the values necessary to meet the PPM peak detector or 468-2 requirements.

The PPM output from voltage-follower IC7a is routed to rectifier selection input IC13/13 and also provides a direct PPM OUT signal on SKT2/3.

13.2.5 Deadband Correction Circuit

The circuit formed by TR1, TR2 and IC8 is designed to reduce rectifier output waveform errors caused by the fact that diodes require a certain minimum conduction voltage for turn-on. In full-wave rectifier circuits this would normally produce a deadband in the zero-crossing region, in which the diode outputs do not follow the input signals.

A 'minimum conduction' voltage is established across D14 by a low current (1.8 μ A approx.) flowing through R31. This voltage is reproduced across R34 by the voltage-follower action of IC8, TR1 and TR2. The current-sharing resistors R32 and R33 ensure that the current flowing in R34 is divided equally between the collector currents flowing in TR1 and TR2. Because the values of R20 and R30 are twice that of R34, the voltage drop across D14 is translated across R20 and R30. This reduces the deadband at the rectifier and peak detector outputs from two 'diode drops' to one. In this way, the

full-wave rectifier waveform distortion is reduced, and the first peak detector efficiency is improved at high frequencies and low levels, thereby reducing level-dependent frequency response errors.

13.2.6 Second Peak Detector

The 468-2 specification calls for two quasi-peak detectors in tandem, the second of which does not need to meet the speed requirements of the first. The second peak detector is a standard version comprising IC9, D9, R45, R46, R89 and C15. The fast-discharge circuits TR3, R44 and TR4, R48, turn on momentarily whenever the MJS401D rectifier is changed to 468-2 in order to rapidly discharge C14 and C15 via R43 and R47 respectively in response to a pulse from the microcomputer. This action prevents the MJS401D meter needle 'pegging' against the right-hand stop when the d.c. gain following the peak detectors is increased when changing from any of the other rectifiers to the 468-2 rectifier.

The 468-2 output is routed to the d.c. amplifier IC7b non-inverting input via R47 and R50 through IC13/14,3.

13.2.7 Average

When average (AVG) is selected, the audio input on SKT1/4 follows the same circuit path through IC1 and the full-wave rectifier stage IC3, IC4, IC5, as described for the PPM rectifier. However, the AVG signal is picked off across C12 and fed via R51 to the rectifier selection multiplexer input IC13/15.

13.2.8 RMS

When RMS is selected, the audio input on SKT1/4 is applied to the amplifier IC1 and then coupled via C7 to the non-inverting input of the low-gain (x4) amplifier IC2b.

The output on IC2b/7 provides the SPEAKER/PHONES output on SKT1/5 and, via C16, supplies the input for the RMS to DC converter, IC10. This provides a d.c. output on IC10/6 that is equivalent to the true r.m.s. value of the input signal. Adjustment of any offset is by preset VR5 connected across the ± 18 V supply rails.

The capacitors C20, C21 together form a second-order low-pass filter in conjunction with an internal voltage follower in IC10 to filter the d.c. output at IC10/6.

The RMS output is routed via R52 to the rectifier selection multiplexer input IC13/12.

13.2.9 Oscilloscope Monitor Output

The MON OUT connector SKT1/6 provides a buffered output for an oscilloscope to monitor the audio input signal, corrected under microcomputer control to remain in phase with the signal input irrespective of the selected function. The buffer amplifier IC2a gives 0.775 V on the monitor output for a 0.775 V (0 dB) reading on the meter. The output level of the monitor can be varied by link LK, which in the LOW position connects R10 across the negative feedback path of IC2a.

The phase of the monitor output is shown non-inverting; i.e. via switch IC12/3,4 and C4 to IC2a/3. This is the condition resulting from a logic 1 on driver input IC12/9 (derived via level shifter IC15/2,3 from the SCOPE MONITOR PHASE input SKT4/3).

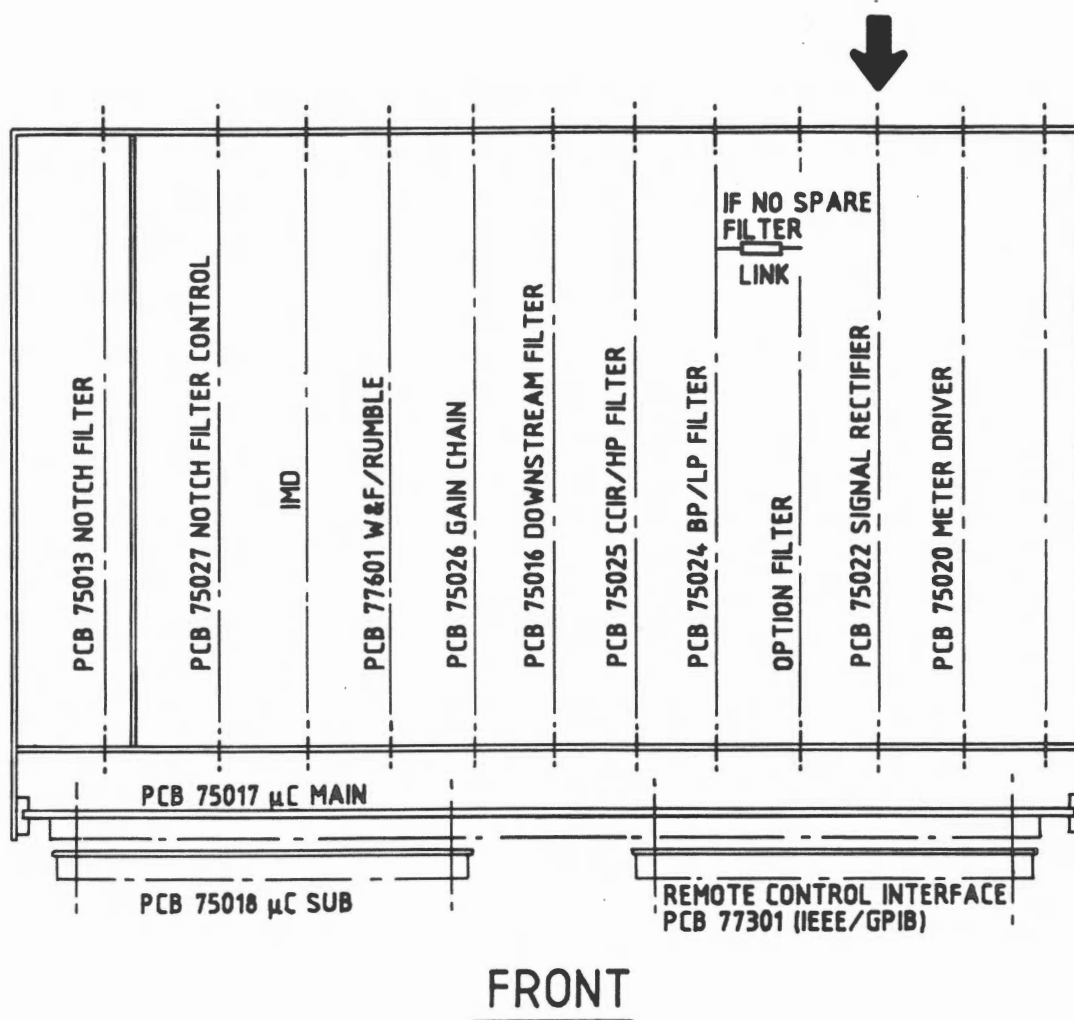
A logic 0 on input SKT4/3 switches C4 to earth via IC12/4,5 and the input signal is routed via R90 and C5 to the inverting input of IC2a to give a phase-inverted monitor output.

13.3 Removal/Replacement

Switch off the MJS401D and remove the mains lead.

Remove the four screws retaining the top cover. Pull the top cover straight up.

With the instrument facing you, the Signal Rectifier card is located in the 10th slot from the left in the main card frame. Verify by noting the printing on the motherboard.



MJS401D PCB Location Guide

Remove the card by grasping the top corners and gently pulling up.

Replacement is the opposite of removal. Carefully line up the connectors before pushing down and ensure the card is properly held within the guides.

Extender card PCB 75031 may be used to facilitate repair and recalibration.

13.4 Fault finding

Use Extender Card PCB 75031.

Status Indicators

Numeric Display

PPM	0
QUASI-PEAK	1
AVG	2
RMS	3
W & F	4
IMD	5
PHASE	6
SPARE	7

<u>Log/Lin status</u>	<u>Log LED</u>	<u>SKT4/1</u>
dB NORM	ON	HIGH
dB EXP	ON	HIGH
% DIST/VOLTS	OFF	LOW

<u>Mon Phase status</u>	<u>Mon Phase LED</u>	<u>SKT4/3</u>
X-TALK, THD	OFF	LOW
LEVEL, READ OSC	ON	HIGH

13.5 Calibration

Use Extender Card PCB75031.

Check D.C. conditions.

IC1	pin 6	+10 mV	to -10 mV
IC2	pin 1	+10 mV	to -10 mV
IC2	pin 7	+10 mV	to -10 mV
D11	cathode	+13.7 V	to +12.3 V
D12	cathode	+5.4 V	to +4.8 V
D10	anode	-4.8 V	to -5.4 V
IC8	pin 2	-17.78 V	to -17.82 V
TR1	emitter	-17.26 V	to -17.4 V
TR2	emitter	same as TR1 emitter	

13.5.1 Check Scope Monitor O/P

Use dual trace scope. Connect the MJS401D "Scope" output to one trace.

If an MD404B Oscillator is fitted:

- Set it to "UNBAL".
- Connect a lead from one "Oscillator" connector to the MJS401D input A and to the other 'scope trace in parallel, taking care to ensure correct phasing of the connection.

If no MD404B is fitted:

- Use an external oscillator.
- Connect the output of the source oscillator to the MJS401D input A and the other 'scope trace in parallel, taking care to ensure correct phasing of the connection.

MJS401D Front Panel Setup

Input	Load	Function	Filters	Rectifier	Scale	Dist'n	Coarse	Fine
A	Off	Level	Off	RMS	dB Norm	---	0	0

Source Setup

Freq	Level	
	dB	V
1 kHz	0	0.775

Confirm 'scope output is in phase with source by observing the scope.

Change "Function" to "X-Talk"

Confirm 'scope output is in phase with source by observing the scope.

Change "function" to "Read Osc"

Confirm 'scope output is in phase with source by observing the scope.

If 'scope MON O/P LEVEL (on PCB 75022 near IC12) is in LOW position (standard) then the 'Scope output should be about x3 (10 dB) lower than the source.

If in the "HIGH" position then it should be about the same as the source level.

13.5.2 Set up input gain

MJS401D Front Panel Setup

Input	Load	Function	Filters	Rectifier	Scale	Dist'n	Coarse	Fine
A	Off	Level	Off	RMS	dB Norm	---	0	0

Source Setup

Freq	LEVEL	
	dB	V
1 kHz	0	0.775

DVM to "MON SCOPE" test point on extender.

Adjust VR1 to read 0.245 V AC on DVM.

(If scope MON O/P is "HIGH" the DVM will read 0.775 V).

13.5.3 Rectifier Gain and Offset Adjustments

MJS401D Front Panel Setup

Input	Load	Function	Filters	Rectifier	Scale	Dist'n	Coarse	Fine
A	Off	Level	Off	RMS	dB Norm	---	0	0

Put DVM on TP3 via a 1 k Ω resistor (this is to prevent the capacitance of the DVM causing IC7b to oscillate).

STEP NO	AUDIO SOURCE	dB COARSE	RECTIFIER	ADJUST	DVM READING
1	OFF	0	RMS	VR5	0 V DC
2	ON	0	RMS	VR9	2.000 V DC
3	OFF	0	QUASI-PEAK	VR3	0.6 V DC approx.
4	ON	+10	QUASI-PEAK	VR2	minimum DC
5	OFF	0	AVG	VR3	0.0 V DC
6	ON	-10	AVG	VR8	6.32 V DC
7	ON	+10	AVG	VR3	0.632 V DC
8	Repeat steps 6 and 7 until they check.				
9	ON	0	AVG	VR8	2.000 V DC
10	OFF	0	QUASI-PEAK	VR4	≈ 0.01 V DC
11	ON	-10	QUASI-PEAK	VR7	6.32 V DC
12	ON	+10	QUASI-PEAK	VR4	0.632 V DC
13	Repeat steps 11 and 12 until they check.				
14	ON	0	QUASI-PEAK	VR7	2.000 V DC
15	ON	0	PPM	VR6	2.000 V DC

13.5.4 Calibrate option inputs

From a low voltage PSU input exactly 1.000 V dc into W&F test point on extender.

Turn test set off.

Depress and hold "LEVEL" while turning on.

Depress "LEVEL" again to get diagnostic Group 1.

Depress "IMD" to get to TEST 3.

Adjust VR10 to give 2.000 V DC with DVM on TP3 via 1 kΩ.

